

FIG. 1

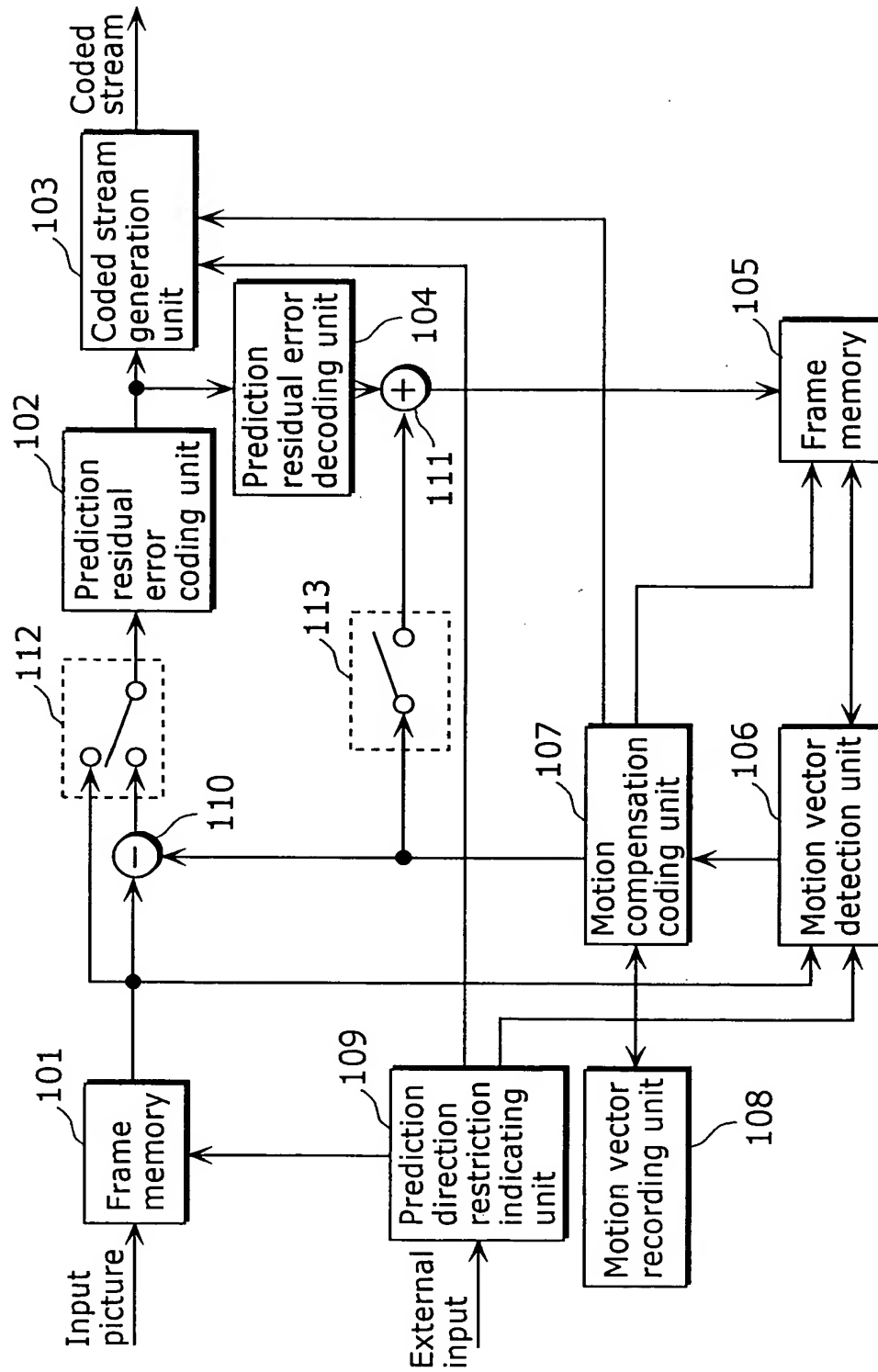


FIG. 2

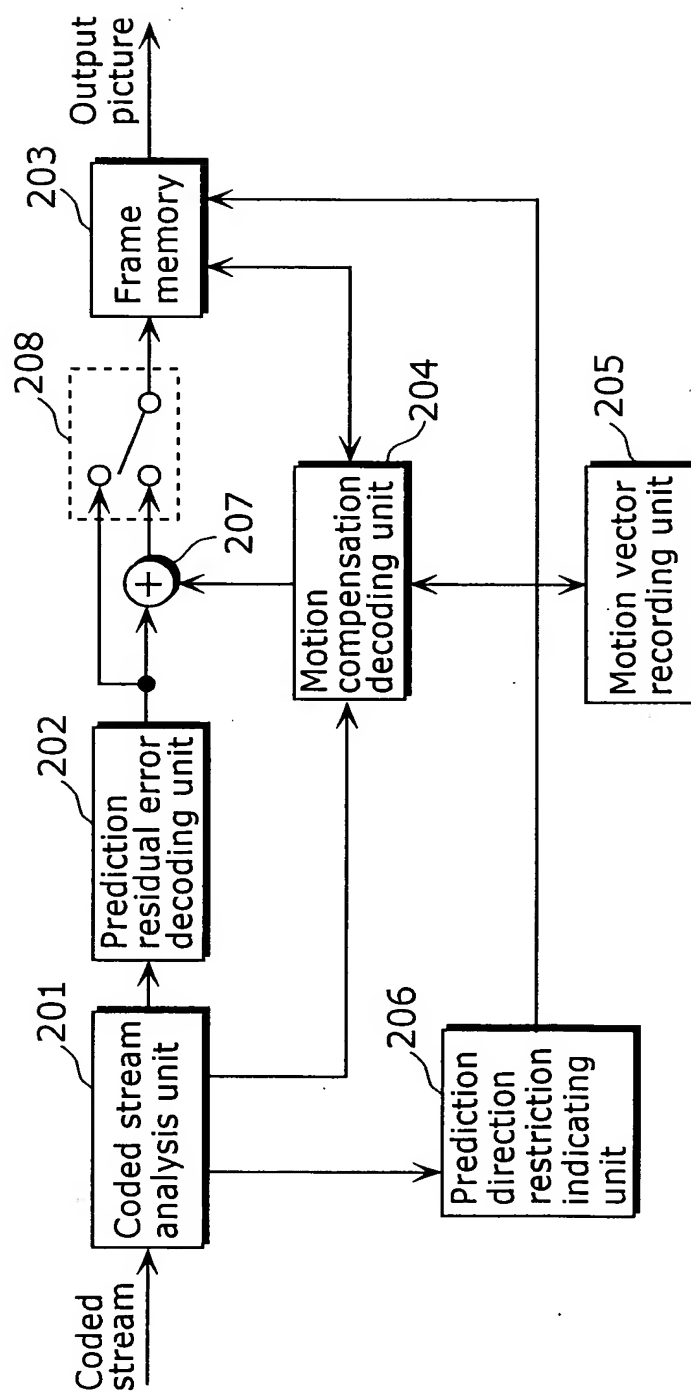


FIG. 3A

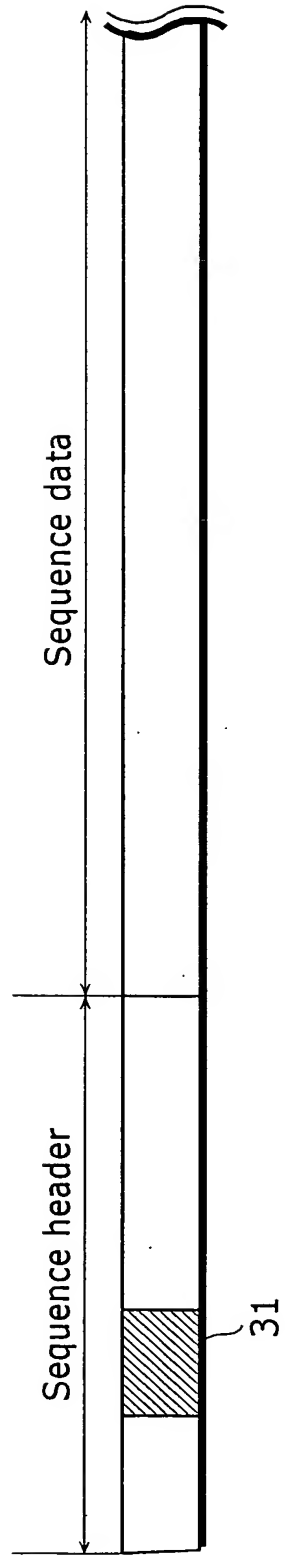


FIG. 3B

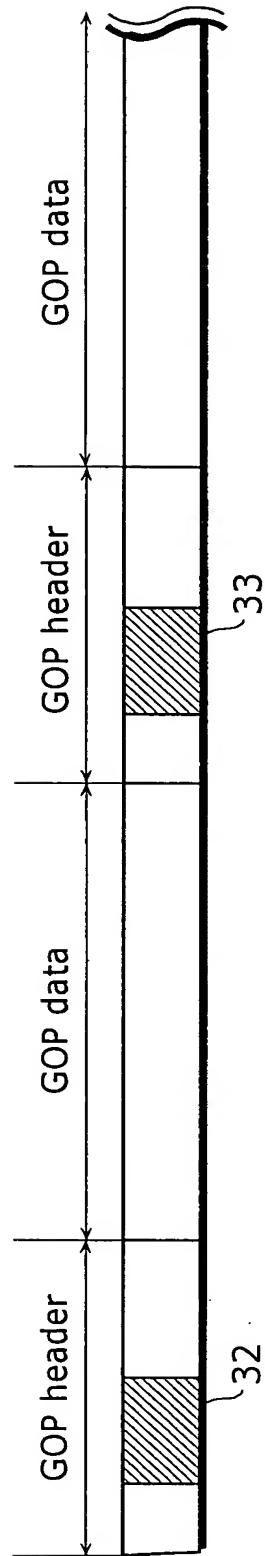


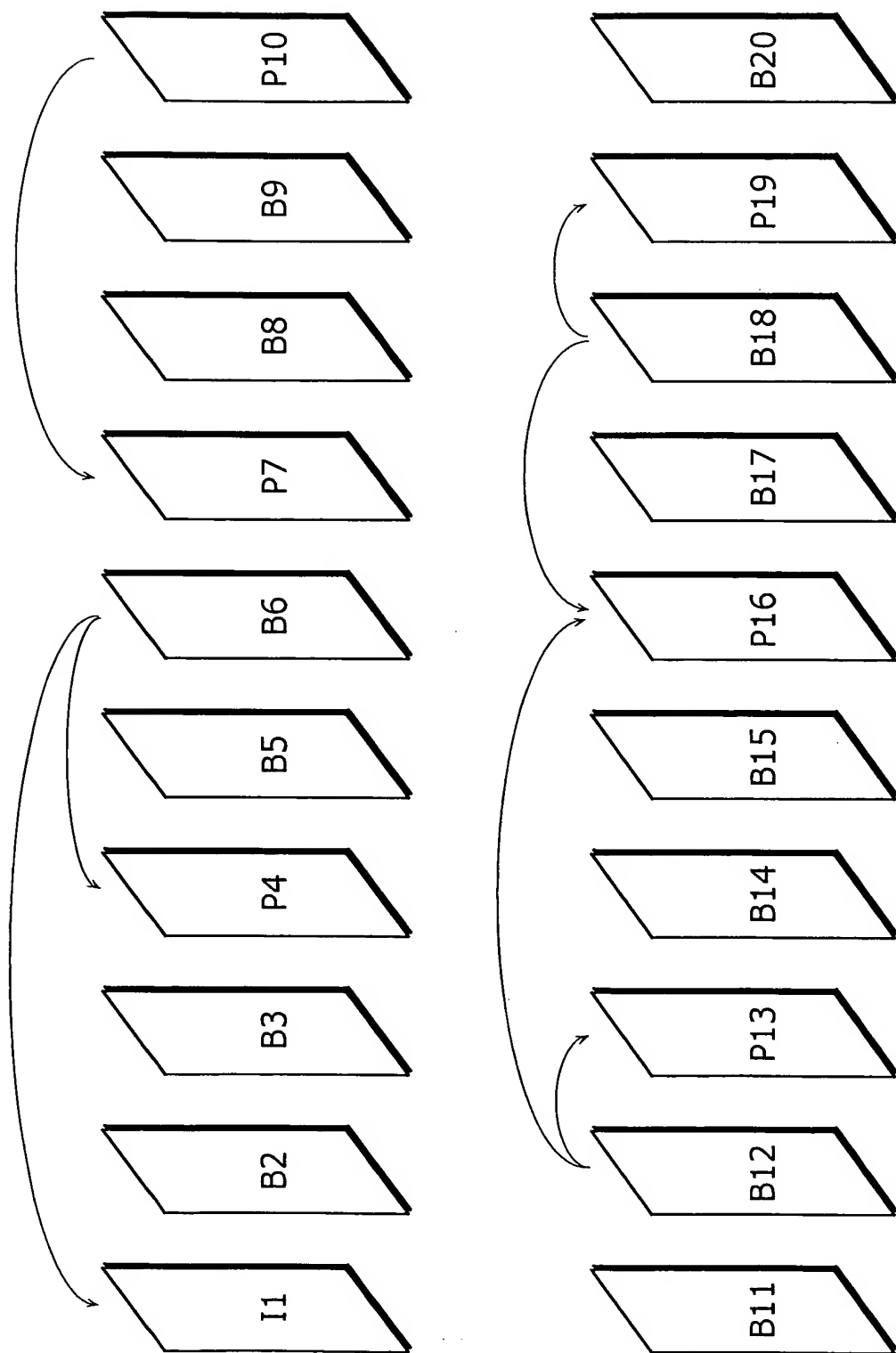
FIG. 4A

Identification number	Usable picture
0	I picture、P picture、B picture
1	I picture、P picture、Forward reference B picture

FIG. 4B

Identification number	Usable picture
0	I picture、P picture、B picture
1	I picture、P picture、Forward reference B picture
2	I picture、P picture

FIG. 5



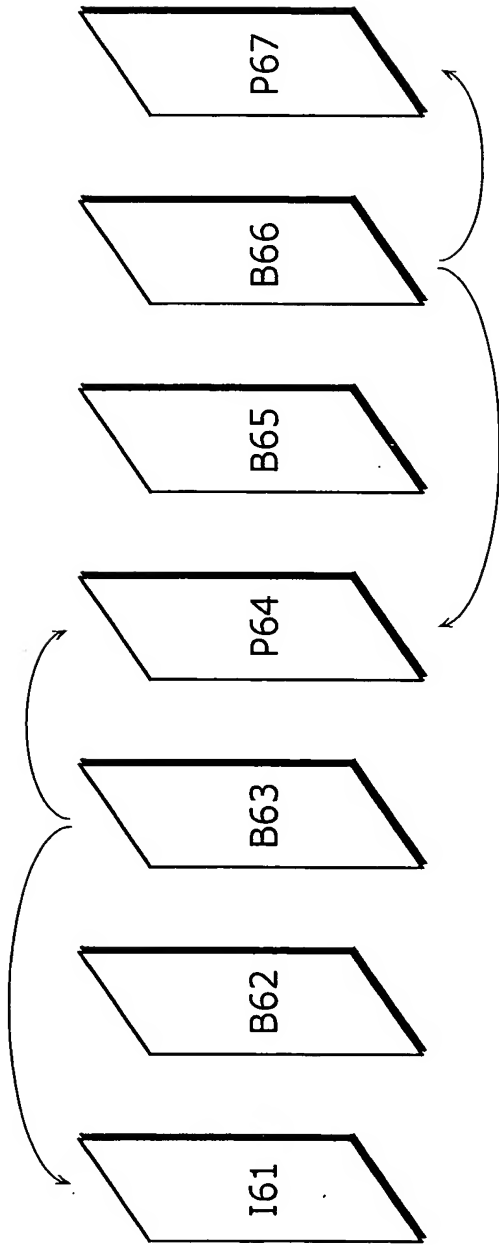


FIG. 6A

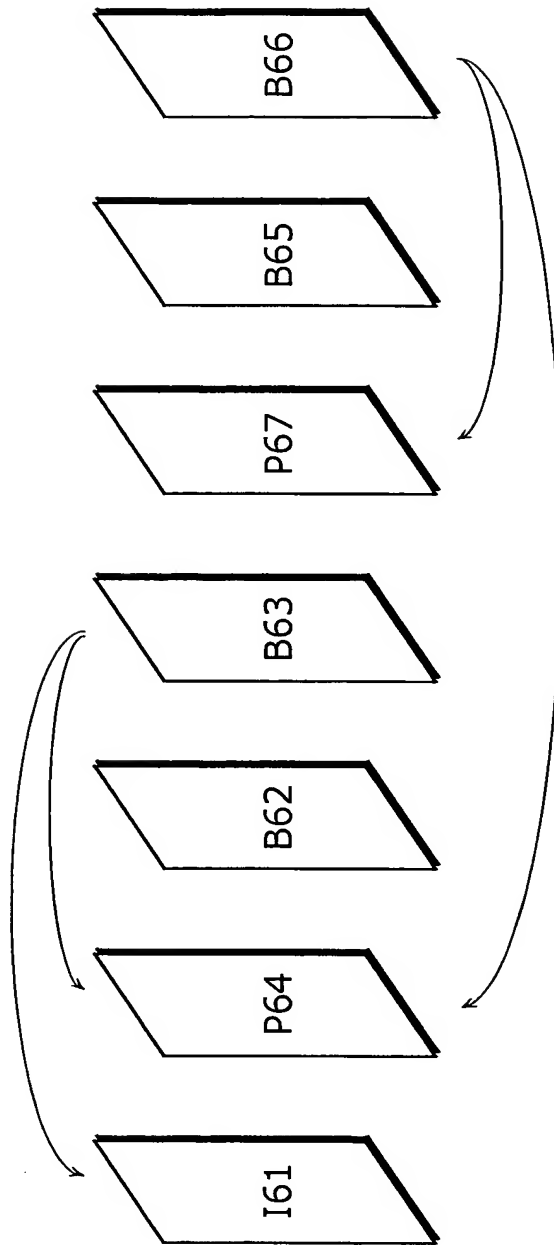


FIG. 6B

FIG. 7

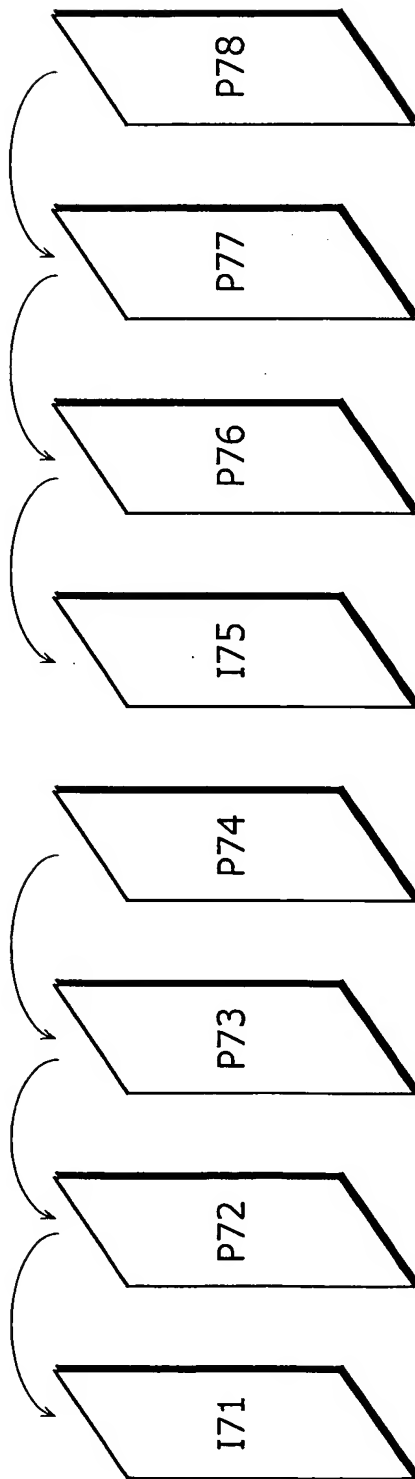


FIG. 8

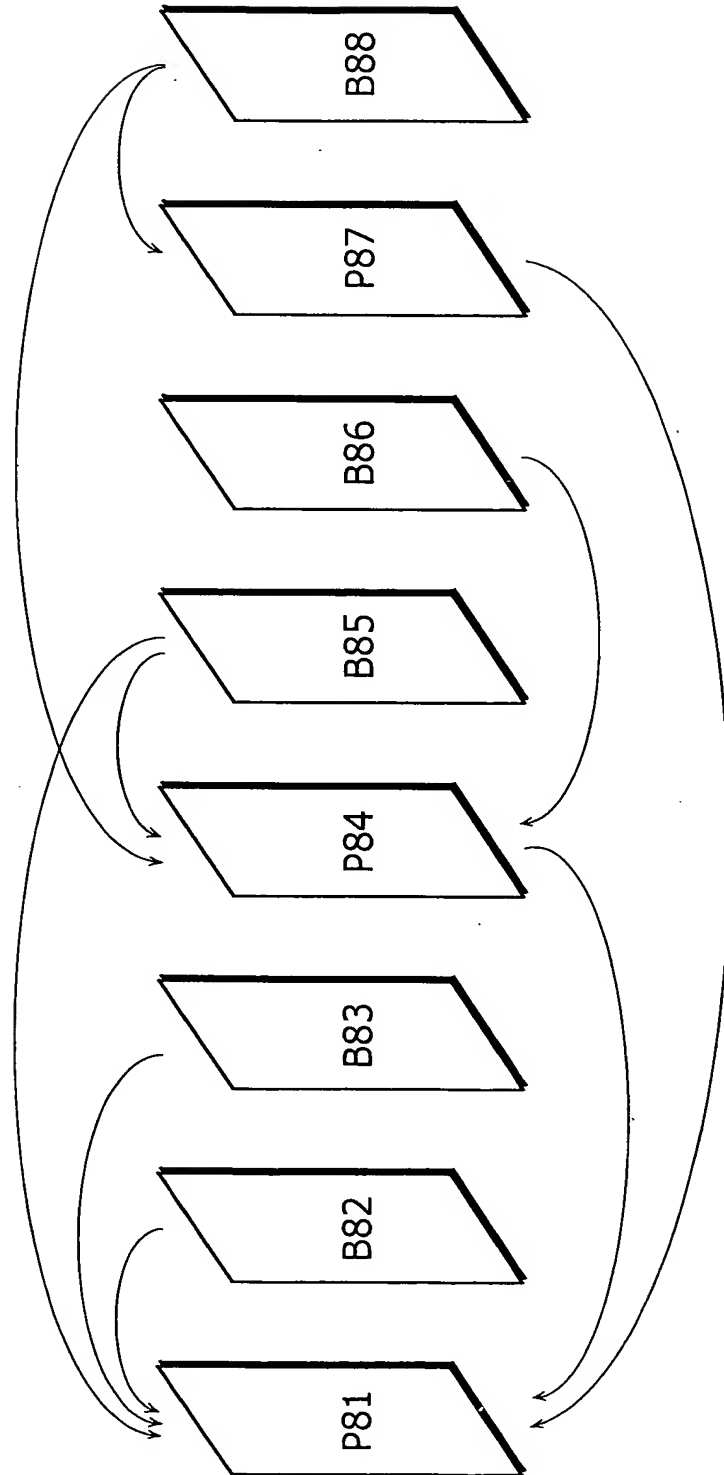


FIG. 9A

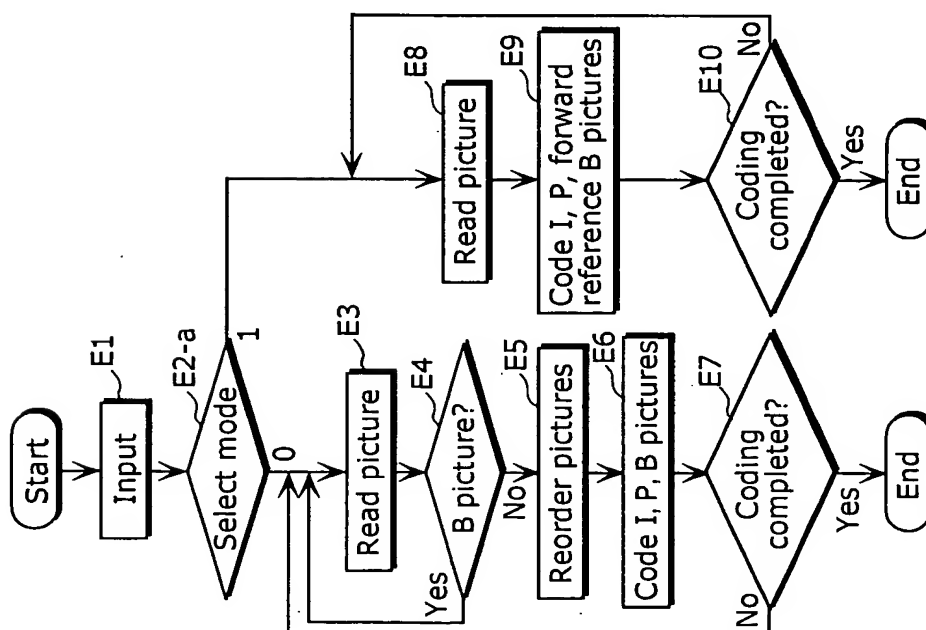


FIG. 9B

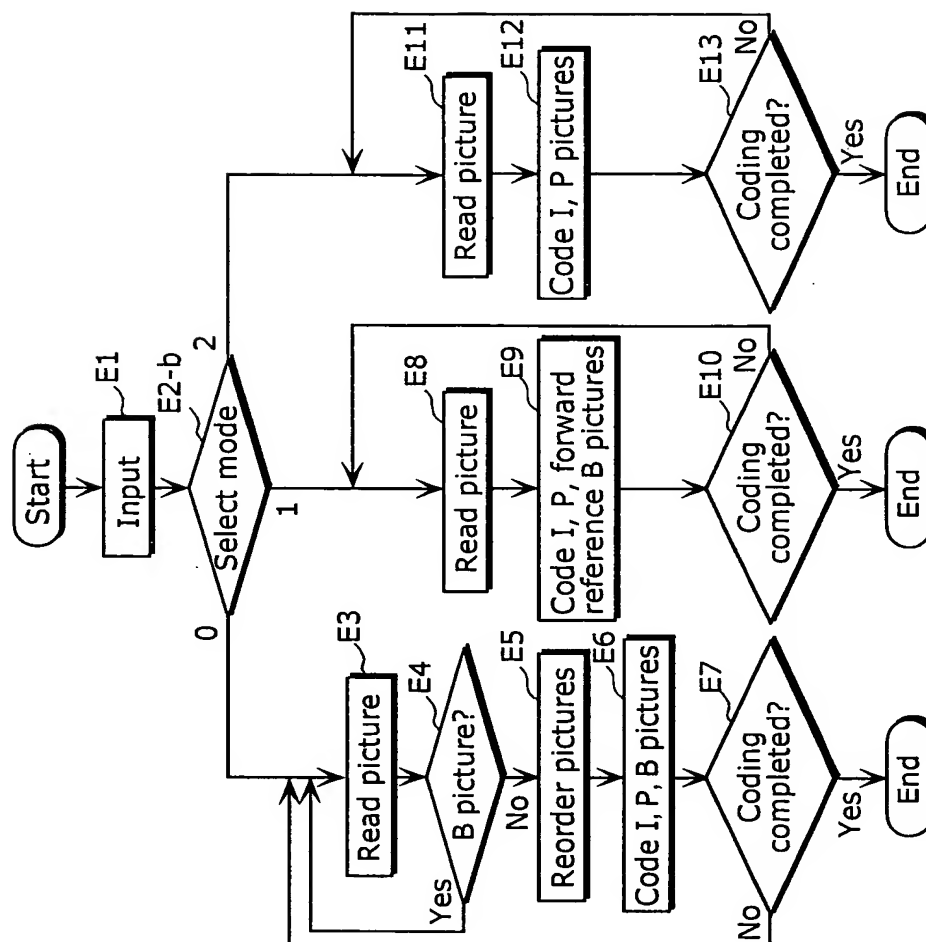


FIG. 10A

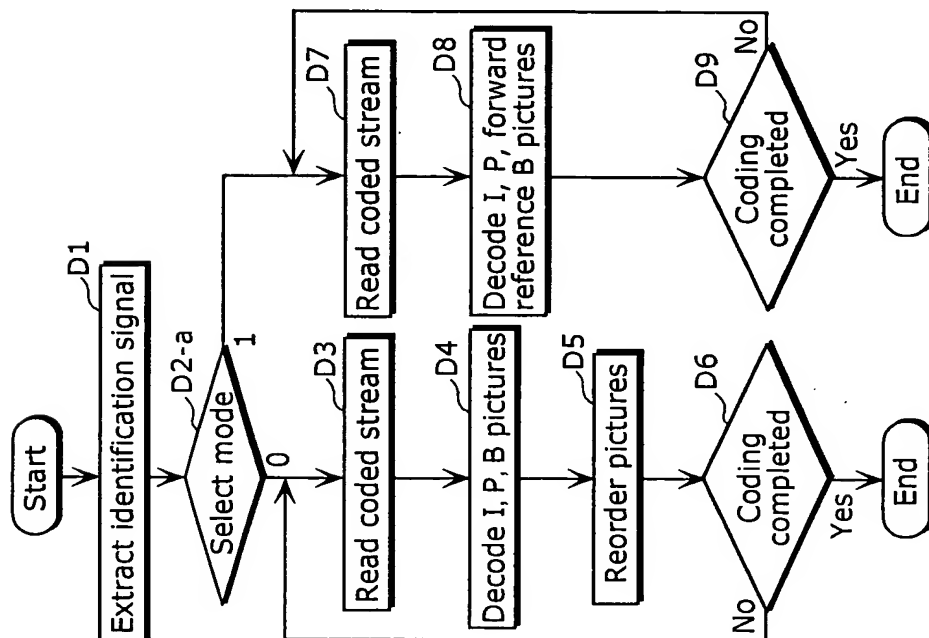


FIG. 10B

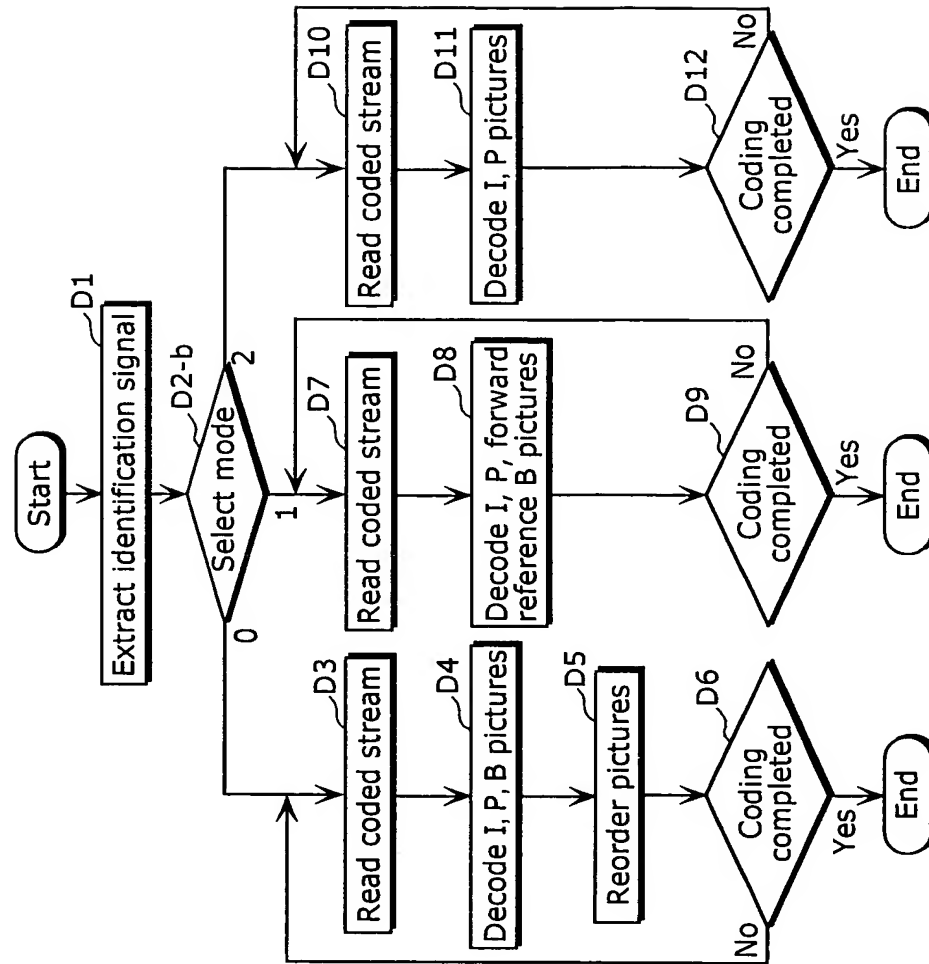


FIG. 11

	Processing amount	Coding efficiency	Delay resistance
I picture, P picture	⊙	△	○
I picture, P picture, Forward reference B picture	○	○	○
I picture, P picture, B picture	△	⊙	△

FIG. 12A

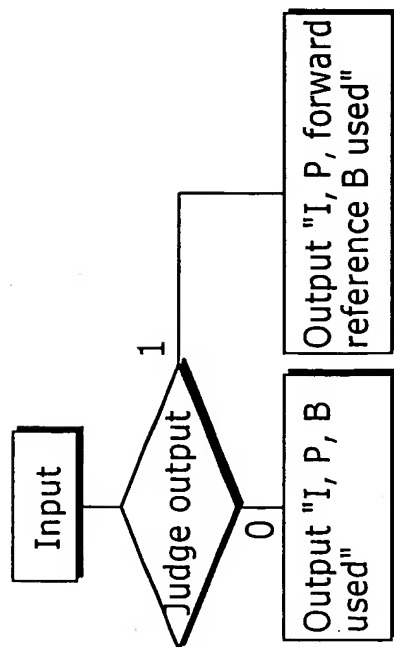


FIG. 12B

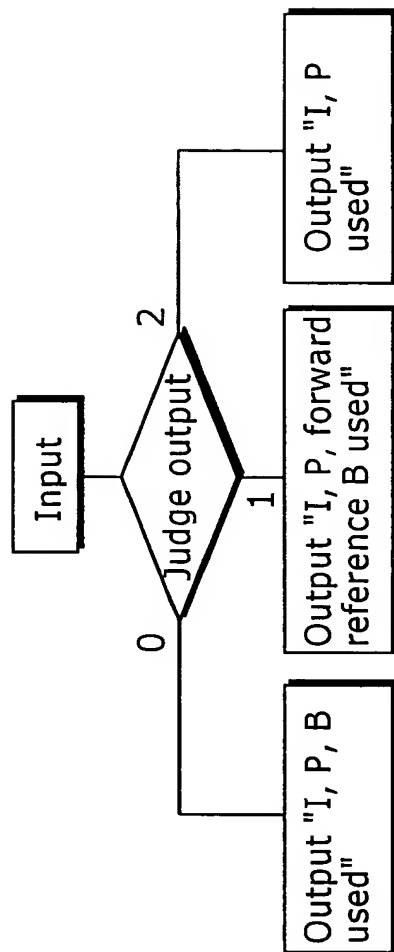


FIG. 12C

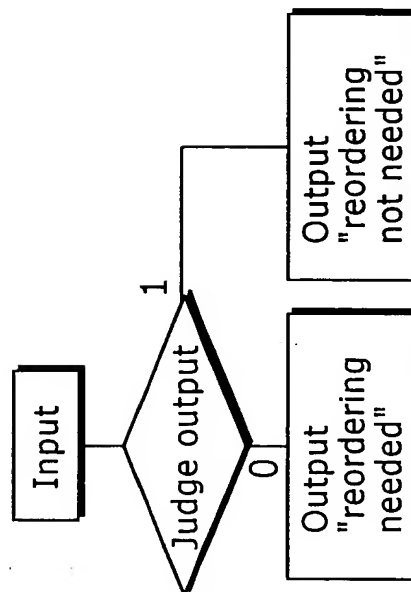


FIG. 12D

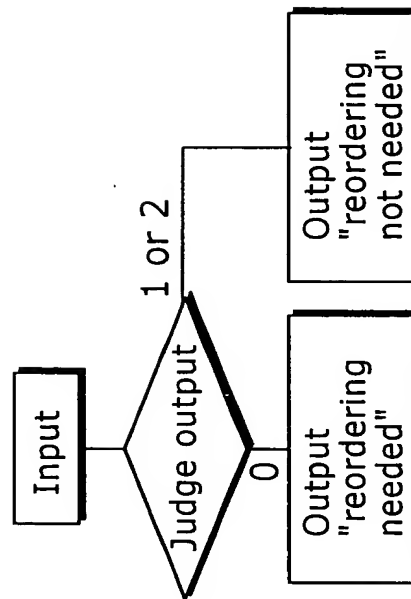


FIG. 13

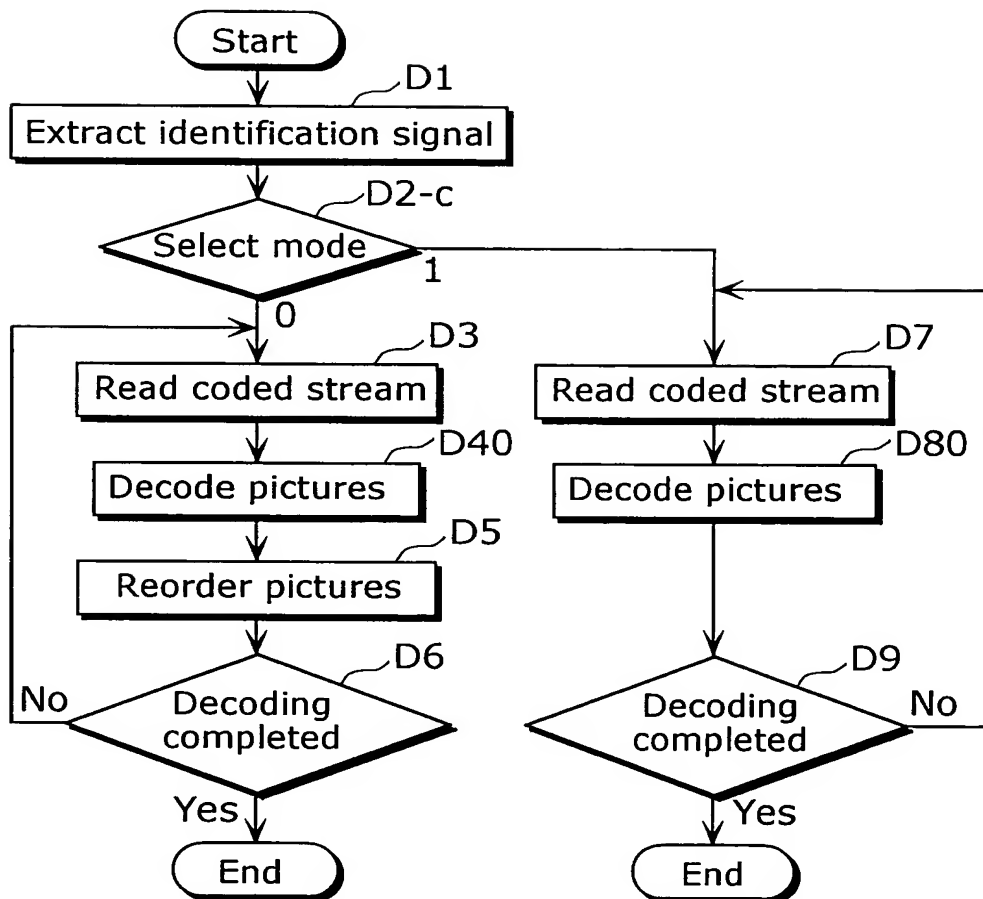


FIG. 14A

Identification number	Used picture
0	I picture、P picture、B picture
1	I picture、P picture、Forward reference B picture

FIG. 14B

Identification number	Used picture
0	I picture、P picture、B picture
1	I picture、P picture、Forward reference B picture
2	I picture、P picture

FIG. 14C

Identification number	Reordering necessity
0	needed
1	not needed

FIG. 15A

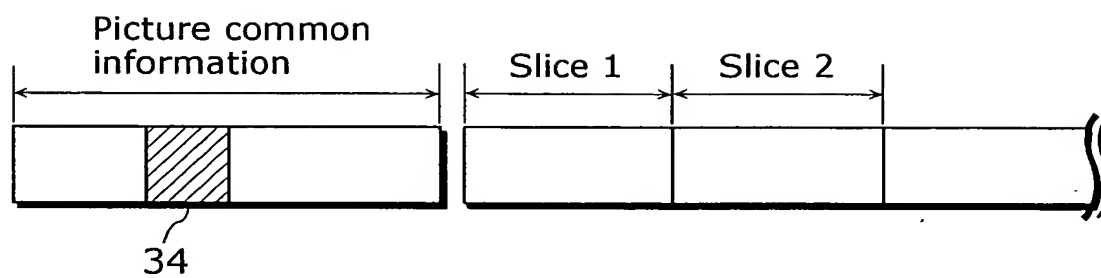
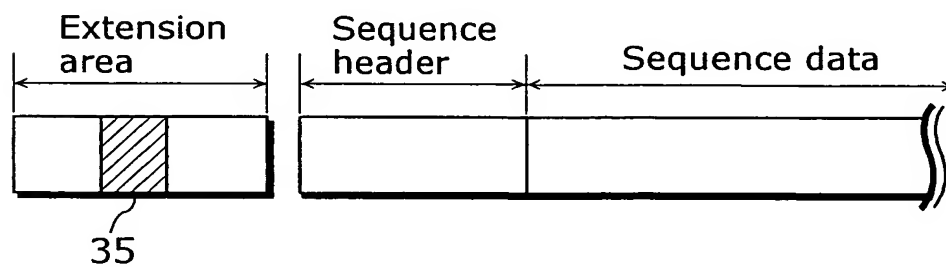
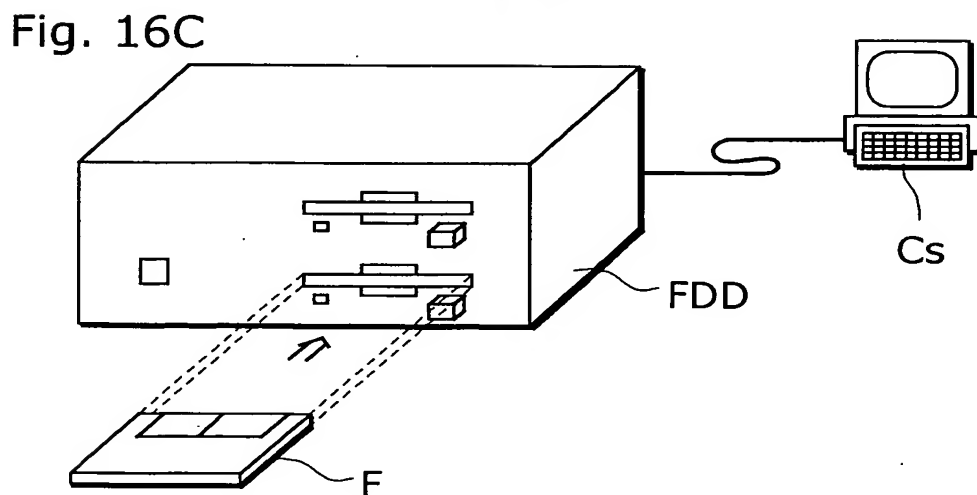
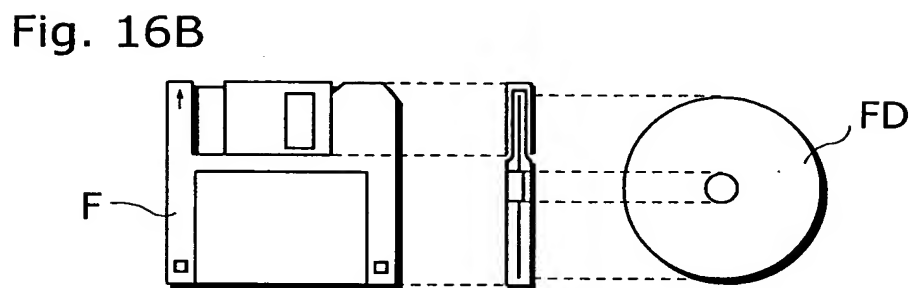
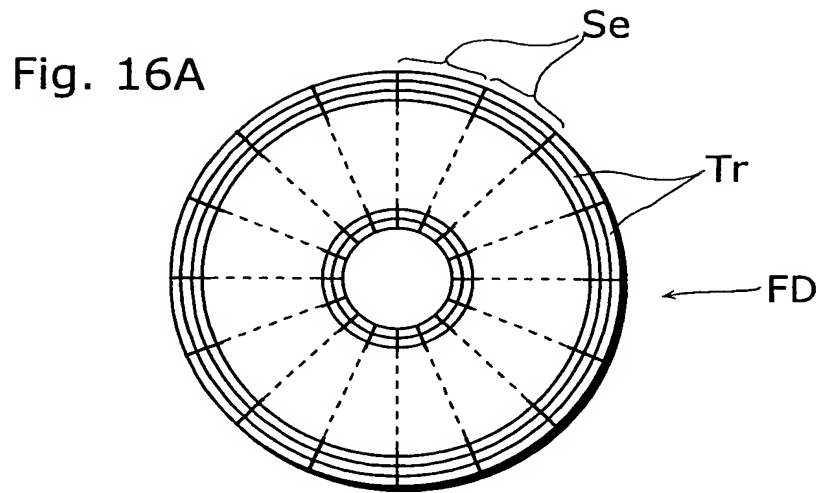


FIG. 15B





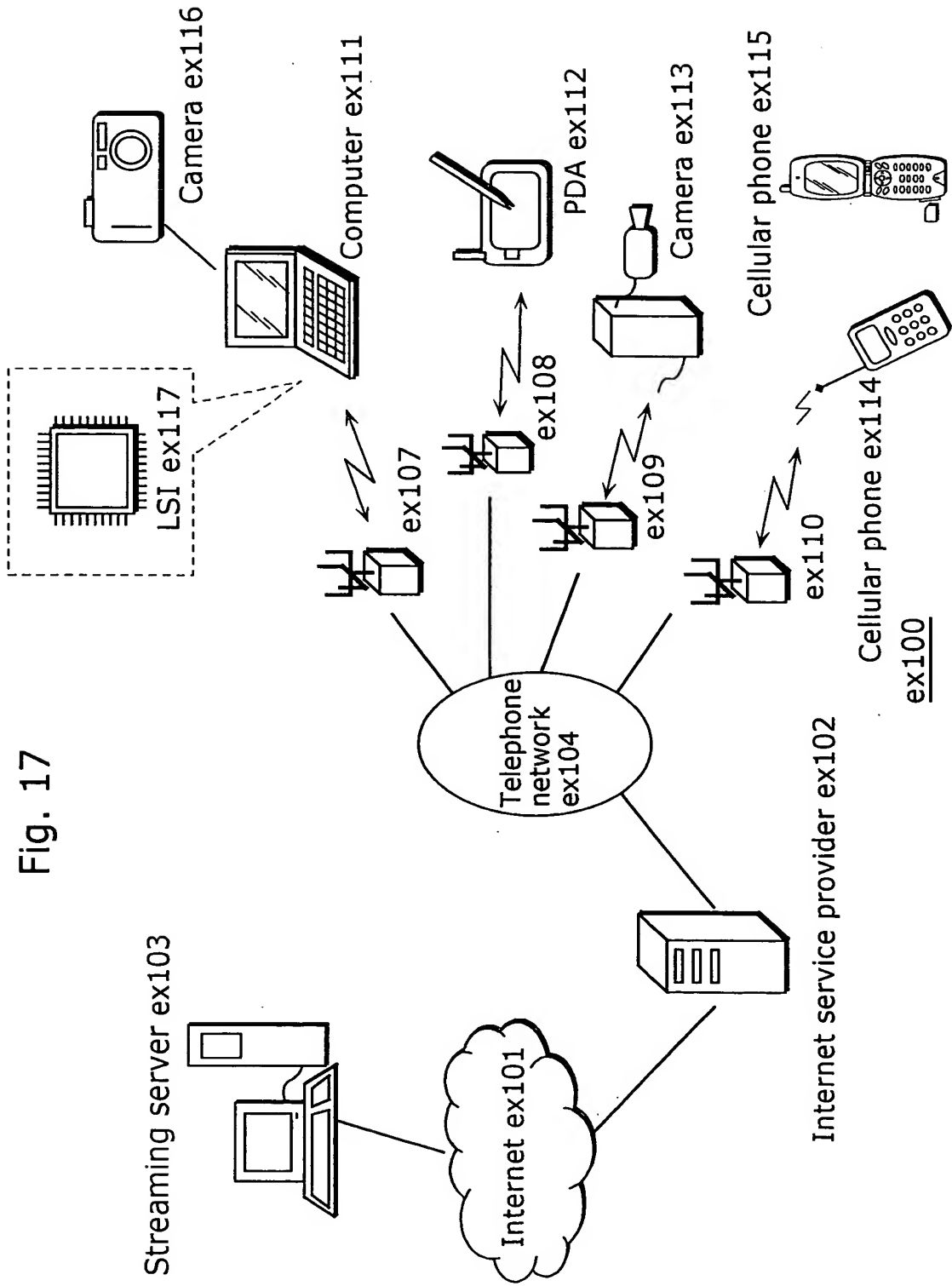


Fig. 17

Fig. 18

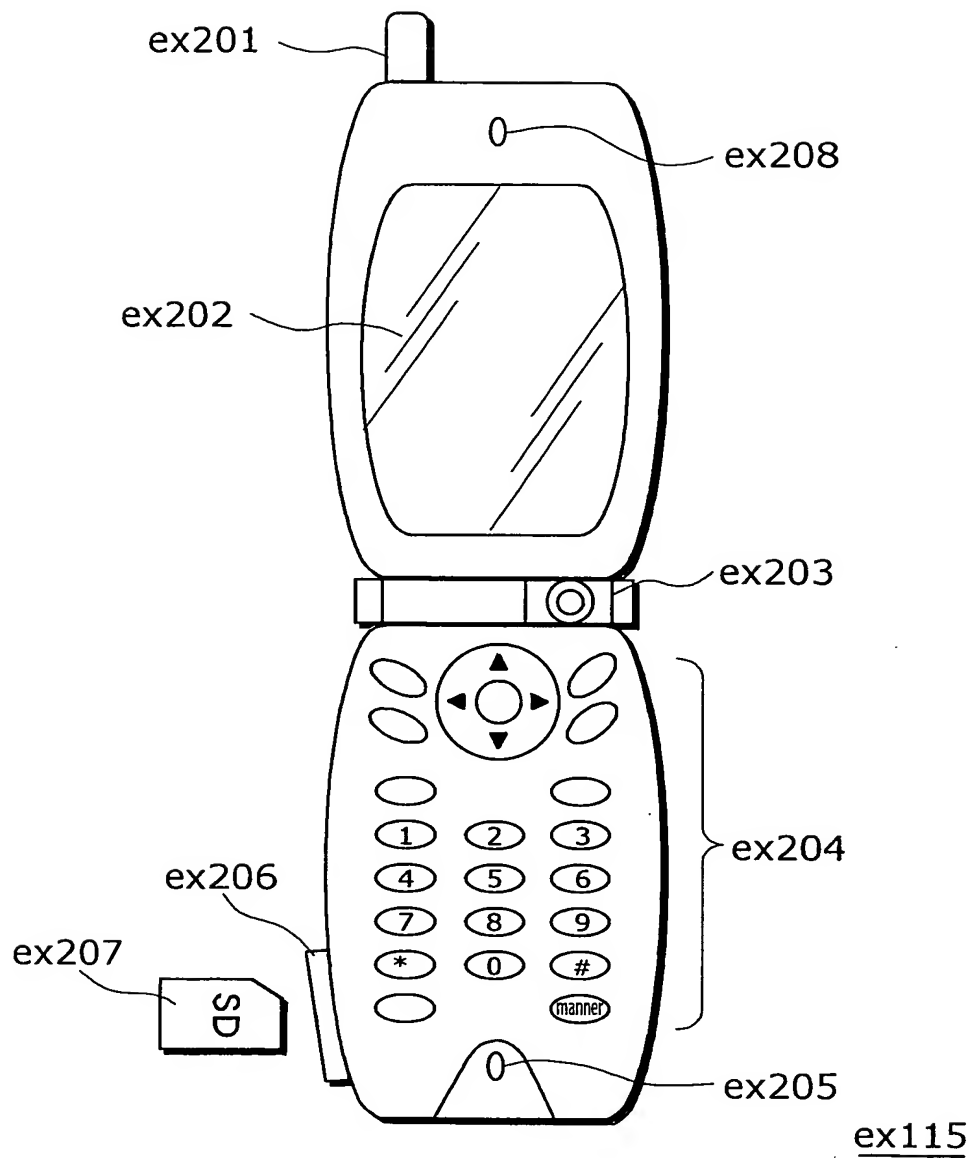


Fig. 19

